REMARKS

This is in response to the Office Action dated July 16, 2003. Examiner's indication that claims 3-14 are allowed is noted with appreciation.

Claims 1 and 2 were rejected under the provisions of 35USC102(e) as being anticipated by Ellis (USP 6,281,724). Claim 1 has been amended to recite that: "a second voltage source coupled to a drain region and a source region of the transistor. This feature is taught by Applicants, for example, at FIG. 2, disclosing Power Regulator 104 coupled to the drain region of transistor 204 by the conductor labeled "Output Voltage" and to the source region of transistor 204 by the common ground connection labeled "Ground". In contradistinction, the second voltage source (labeled "15" in FIG. 3 of Ellis) is connected only to the drain region of transistor 30. The source region of transistor 30 is NOT coupled to the second voltage source. Rather, the source region of transistor 30 is coupled to first voltage source 13.

The foregoing amendment to claim 1 is believed to overcome the rejection under 35USC 102(e). For this reason, claim 1, as amended, is believed to be allowable. Claim 2 is dependent on Claim 1 and is believed to be allowable for the same reason and that it recites additional features of the invention.

Newly added claim 15 recites: A transient load generator for testing a microelectronic power delivery system, the generator comprising: a first voltage source having a first output voltage, a control circuit coupled to the first voltage source, a transistor having a gate region coupled to the control circuit, and a second voltage source having a second output voltage coupled to a drain region of the transistor, wherein the second output voltage is greater than the first output voltage. (The underlined portions are intended to show distinctions over previously rejected claim 1.) The cited references in general and the Ellis (USP 6,281,724) reference specifically fails to teach such a structure. Rather, Ellis discloses (at FIG. 3) that the first voltage source 13 provides +12v and that the second voltage source 15 provides +5v such that the

second voltage (+5v) is smaller than the first voltage (+12v). Accordingly, Ellis teaches away from Applicants' invention, rather than anticipating Applicants' invention, as succinctly set forth in claim 15.

For the foregoing reasons, newly added claim 15 is believed allowable. Similarly, claim 16, dependent on claim 15, is also believed to be allowable. Newly added claim 17, dependent on claim 15, is also believed to be allowable for the same reasons and in that it further recites that the transistor is an N Channel Field Effect Transistor. Note that Ellis specifically illustrates a P Channel Field Effect Transistor 30 (FIG. 3), further described as PMOS transistor 30 at column 5, line 14.

In conclusion, all of the claims (1-17) remaining in this application are believed to be allowable. Amended claim 1 and newly added independent claim 15 have been shown to be patentably distinct from the cited references, in particular the Ellis patent. Dependent claims 2, 16, and 17 are believed allowable for the same reasons and that they recite additional features of the invention. Claims 3-14 were allowed and warrant no further discussion.

In view of the foregoing, it is believed that all the claims currently in this application are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
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